

Claims

- [c1] **1. A silicon-on-insulator radiation detector, comprising:**
a silicon layer formed on an insulating substrate,
wherein the silicon layer includes a PNPN structure;
a gate layer formed over the PNPN structure, wherein the
gate layer includes a PN gate; and
wherein latch-up occurs in the radiation detector only in
response to incident radiation.
- [c2] **The silicon-on-insulator radiation detector of claim 1,**
wherein the PNPN structure comprises a P+ region, an
N-well, a P-well, and an N+ region, and wherein the PN
gate comprises a first P+ region and a first N+ region.
- [c3] **The silicon-on-insulator radiation detector of claim 2,**
wherein the first P+ region of the gate covers the N-well
of the PNPN structure and extends a substantial distance
over the P-well of the PNPN structure.
- [c4] **The silicon-on-insulator radiation detector of claim 3,**
further comprising:
a parasitic PMOS FET within the radiation detector that is
prevented from turning on by coupling the P+ region of
the PNPN structure and the first P+ region of the gate to

a source voltage; and
a parasitic NMOS FET within the radiation detector having a threshold voltage of about 1.2 volts, wherein the threshold voltage prevents the parasitic NMOS FET from turning on.

- [c5] The silicon-on-insulator radiation detector of claim 2, wherein the first N+ region of the gate covers the P-well of the PNPN structure and extends a substantial distance over the N-well of the PNPN structure.
- [c6] The silicon-on-insulator radiation detector of claim 5, further comprising:
 - a parasitic NMOS FET within the radiation detector that is prevented from turning on by coupling the N+ region of the PNPN structure and the first N+ region of the gate to ground; and
 - a parasitic PMOS FET within the radiation detector having a threshold voltage of about -1.2 volts, wherein the threshold voltage prevents the parasitic PMOS FET from turning on.
- [c7] The silicon-on-insulator radiation detector of claim 1, wherein the gate layer comprises a PNPN gate, and wherein the PNPN gate includes a first P+ region, a first N+ region, a second P+ region, and a second N+ region.

- [c8] The silicon-on-insulator radiation detector of claim 7, wherein the first N+ region of the PNPN gate is located over the N-well of the PNPN structure and the second P+ region of the PNPN gate is located over the P-well of the PNPN structure.
- [c9] The silicon-on-insulator radiation detector of claim 8, wherein an interface between the first N+ region and the second P+ region of the PNPN gate is substantially coincident with an interface between the P-well and N-well of the PNPN structure.
- [c10] The silicon-on-insulator radiation detector of claim 8, further comprising:
 - a parasitic PMOS FET within the radiation detector having a threshold voltage of about -1.2 volts, wherein the threshold voltage prevents the parasitic PMOS FET from turning on; and
 - a parasitic NMOS FET within the radiation detector having a threshold voltage of about 1.2 volts, wherein the threshold voltage prevents the parasitic NMOS FET from turning on.
- [c11] 11. A radiation detector, comprising:
 - a silicon-on-insulator PNPN diode structure, wherein latch-up occurs in the radiation detector only in response to incident radiation.

- [c12] The radiation detector of claim 11, further comprising:
a PN gate over the PNPN diode structure, wherein at least one parasitic FET within the radiation detector has a threshold voltage of about 1.2 volts or -1.2 volts.
- [c13] The radiation detector of claim 11, further comprising:
a PNPN gate over the PNPN diode structure, wherein at least one parasitic FET within the radiation detector has a threshold voltage of about 1.2 volts or -1.2 volts.
- [c14] 14. An integrated circuit, comprising:
a silicon-on-insulator radiation detector, wherein the radiation detector includes:
a silicon layer formed on an insulating substrate,
wherein the silicon layer includes a PNPN structure;
a gate layer formed over the PNPN structure, wherein the gate layer includes a PN gate; and
wherein latch-up occurs in the radiation detector only in response to incident radiation.
- [c15] The integrated circuit of claim 14, wherein the PNPN structure comprises a P+ region, an N-well, a P-well, and an N+ region, wherein the PN gate comprises a first P+ region and a first N+ region, and wherein the first P+ region of the gate covers the N-well of the PNPN structure and extends a substantial distance over the P-well

of the PNPN structure.

- [c16] The integrated circuit of claim 14, wherein the PNPN structure comprises a P+ region, an N-well, a P-well, and an N+ region, wherein the PN gate comprises a first P+ region and a first N+ region, and wherein the first N+ region of the gate covers the P-well of the PNPN structure and extends a substantial distance over the N-well of the PNPN structure.